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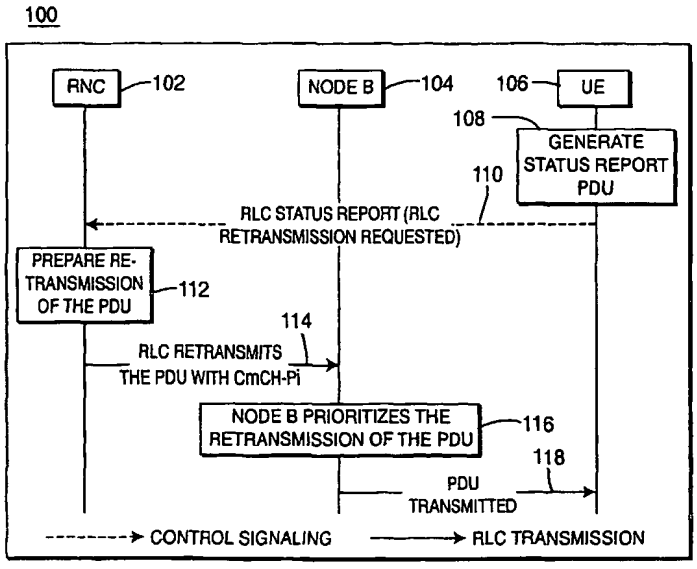
(54) Title: SYSTEM AND METHOD FOR PRIORITIZATION OF RETRANSMISSION OF PROTOCOL DATA UNITS TO ASSIST RADIO-LINK-CONTROL RETRANSMISSION



(57) Abstract: A medium access control (MAC) architecture reduces transmission latency for data block retransmissions. A plurality of data blocks are received and temporarily stored in a first memory (e.g., queue, buffer). The plurality of data blocks are then transmitted. A determination is made as to whether each of the transmitted data blocks was received successfully or needs to be retransmitted because the data block was not received successfully. Each of the transmitted data blocks that needs to be retransmitted is marked and temporarily stored in a second memory having a higher priority than the first memory. The marked data blocks are retransmitted before data blocks stored in the first memory location.

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[0001] # SYSTEM AND METHOD FOR PRIORITIZATION OF RETRANSMISSION OF PROTOCOL DATA UNITS TO ASSIST RADIO-LINK-CONTROL RETRANSMISSION

[0002] ## FIELD OF THE INVENTION

[0003] The present invention relates to the field of wireless communications. More specifically, the present invention relates to a system and method for prioritizing the retransmission of protocol data units (PDUs) to assist radio link control (RLC) layer retransmission.

[0004] ## BACKGROUND

[0005] In third generation (3G) cellular systems for Frequency Division Duplex (FDD) and Time Division Duplex (TDD), there are retransmission mechanisms in the Acknowledgement Mode of the Radio Link Control (RLC) layer to achieve high reliability of end-to-end data transmissions. The RLC layer is a peer entity in both the Radio Network Controller (RNC) and the User Equipment (UE).

[0006] A block diagram of a UMTS Terrestrial Radio Access Network (UTRAN) MAC-hs layer architecture is illustrated in Figure 1, and a block diagram of the user equipment (UE) MAC hs architecture is shown in Figure 2. The architecture shown in Figures 1 and 2 is described in detail co-pending U.S. patent application number 10/270,822 filed on October 15, 2002 which is assigned to the present assignee. The UTRAN MAC-hs 30 shown in Figure 1 comprises a transport format resource indicator (TFRI) selector 31, a scheduling and prioritization entity 32, a plurality of Hybrid Automatic Repeat (H-ARQ) processors 33a, 33b, a flow controller 34 and a priority class and transmission sequence number (TSN) setting entity 35.

[0007] The UE MAC-hs 40 comprises an H-ARQ processor 41. As will be explained with reference to both Figures 1 and 2, the H-ARQ processors 33a, 33b in the UTRAN MAC-hs 30 and the H-ARQ processor 41 in the UE MAC-hs 40 work together to process blocks of data.

[0008] The H-ARQ processors 33a, 33b in the UTRAN MAC-hs 30 handle all of the tasks that are required for the H-ARQ process to generate transmissions and retransmissions for any transmission that is in error. The H-ARQ processor 41 in the UE MAC-hs 40 is responsible for generating an acknowledgement (ACK) to indicate a successful transmission, and for generating a negative acknowledgement (NACK) to indicate a failed transmission. The H-ARQ processors 33a, 33b and 41 process sequential data streams for each user data flow.

[0009] As will be described in further detail hereinafter, blocks of data received on each user data flow are assigned to H-ARQ processors 33a, 33b. Each H-ARQ processor 33a, 33b initiates a transmission, and in the case of an error, the H-ARQ processor 41 requests a retransmission. On subsequent transmissions, the modulation and coding rate may be changed in order to ensure a successful transmission. The data block to be retransmitted and any new transmissions to the UE are provided by the scheduling and prioritization entity 32 to the H-ARQ entities 33a, 33b.

[00010] The scheduling and prioritization entity 32 functions as radio resource manager and determines transmission latency in order to support the required QoS. Based on the outputs of the H-ARQ processors 33a, 33b and the priority of a new data block being transmitted, the scheduling and prioritization entity 32 forwards the data block to the TFRI selector 31.

[00011] The TFRI selector 31, coupled to the scheduling and prioritization entity 32, receives the data block to be transmitted and selects an appropriate dynamic transport format for the data block to be transmitted. With respect to H-ARQ transmissions and retransmissions, the TFRI selector 31 determines modulation and coding.

[00012] It is highly desirable for the retransmitted data blocks to arrive at the RLC entity of the receiving side (i.e., the UE) as soon as possible for several reasons. First, the missed data block will prevent subsequent data blocks from being forwarded to higher layers, due to the requirement of in-sequence delivery. Second, the buffer of the UE needs to be sized large enough to accommodate the

latency of retransmissions while still maintaining effective data rates. The longer the latency is, the larger the UE buffer size has to be to allow for the UE to buffer both the data blocks that are held up and continuous data receptions until the correct sequence data block is forwarded to higher layers. The larger buffer size results in increased hardware costs for UEs. This is very undesirable.

[00013] Referring to Figure 3, a simplified flow diagram of the data flow between a Node B (shown at the bottom of Figure 3) and a UE (shown at the top of Figure 3) is shown. PDUs from higher level processing are scheduled and may be multiplexed into one data block. A data block can only contain PDUs of higher layers of the same priority. A unique TSN is assigned to each data block by the scheduler. The higher layers may provide a plurality of streams of different priorities of PDUs, each priority having a sequence of TSNs. The scheduler then dispatches the data blocks to the plurality of H-ARQ processors $P1_B$-$P5_B$. Each H-ARQ processor $P1_B$-$P5_B$ is responsible for processing a single data block at a time. For example, as shown in Figure 3, the Priority 1 PDUs comprise a sequence illustrated as $B1_1$-$B1_N$. Likewise, the Priority 2 PDUs are sequenced from $B2_1$-$B2_N$ and the Priority 3 PDUs are sequenced from $B3_1$-$B3_N$. These PDUs are scheduled (and may be multiplexed) and affixed a TSN by the common scheduler. For purposes of describing the invention, it is assumed that one PDU equals one data block. After a data block is scheduled to be processed by a particular processor $P1_B$-$P5_B$, each data block is associated with a processor identifier, which identifies the processor $P1_B$-$P5_B$ that processes the data block.

[00014] The data blocks are then input into the scheduled Node B H-ARQ processors $P1_B$-$P5_B$ which receive and process each data block. Each Node B H-ARQ processor $P1_B$-$P5_B$ corresponds to an H-ARQ processor $P1_{UE}$-$P5_{UE}$ within the UE. Accordingly, the first H-ARQ processor $P1_B$ in the Node B communicates with the first H-ARQ processor $P1_{UE}$ in the UE. Likewise, the second H-ARQ processor $P2_B$ in the Node B communicates with the second H-ARQ processor $P2_{UE}$ in the UE, and so on for the remaining H-ARQ processors $P3_B$-$P5_B$ in the Node B and their counterpart H-ARQ processors $P3_{UE}$-$P5_{UE}$ respectively within

the UE. The H-ARQ processes are timely multiplexed onto the air interface and there is only one transmission of an H-ARQ on the air interface at one time.

[00015] For example, taking the first pair of communicating H-ARQ processors $P1_B$ and $P1_{UE}$, the H-ARQ processor $P1_B$ processes a data block, for example $B1_1$, and forwards it for multiplexing and transmitting it over the air interface. When this data block $B1_1$ is received by the first H-ARQ processor $P1_{UE}$, the processor $P1_{UE}$ determines whether or not it was received without error. If the data block $B1_1$ was received without error, the first H-ARQ processor $P1_{UE}$ transmits an ACK to indicate to the transmitting H-ARQ processor $P1_B$ that it has been successfully received. On the contrary, if there is an error in the received data block $B1_1$, the receiving H-ARQ processor $P1_{UE}$ transmits a NACK to the transmitting H-ARQ processor $P1_B$. This process continues until the transmitting processor $P1_B$ receives an ACK for the data block $B1_1$. Once an ACK is received, that processor $P1_B$ is "released" for processing another data block. The scheduler will assign the processor $P1_B$ another data block if available, and can choose to retransmit or start a new transmission at any time.

[00016] Once the receiving H-ARQ processors $P1_{UE}$-$P5_{UE}$ process each data block, they are forwarded to the reordering buffers R_1, R_2, R_3 based on their priority; one reordering buffer for each priority level of data. For example, Priority 1 data blocks $B1_1$-$B1_N$ will be received and reordered in the Priority 1 reordering buffer R_1; Priority 2 data blocks $B2_1$-$B2_N$ will be received and reordered in the Priority 2 reordering buffer R_2; and the Priority 3 data blocks $B3_1$-$B3_N$ will be received and reordered by the Priority 3 reordering buffer R_3.

[00017] Due to the pre-processing of the data blocks by the receiving H-ARQ processors $P1_{UE}$-$P5_{UE}$ and the ACK/NACK acknowledgement procedure, the data blocks are often received in an order that is not sequential with respect to their TSNs. The reordering buffers R_1-R_3 receive the out-of-sequence data blocks and attempt to reorder the data blocks in a sequential manner prior to forwarding onto the RLC layer. For example, the Priority 1 reordering buffer R_1 receives and reorders the first four Priority 1 data blocks $B1_1$-$B1_4$. As the data blocks are received and reordered, they will be passed to the RLC layer.

[00018] On the receiving side, the UE MAC-hs, (which has been graphically illustrated as MAC-hs control), reads the H-ARQ processor ID, whether it is sent on a control channel such as the HS-SCCH or whether the data block has been tagged, to determine which H-ARQ processor $P1_{UE}$-$P5_{UE}$ has been used. If the UE receives another data block to be processed by the same H-ARQ processor $P1_{UE}$-$P5_{UE}$, the UE knows that that particular H-ARQ processor $P1_{UE}$-$P5_{UE}$ has been released regardless of whether or not the previous data block processed by that H-ARQ processor $P1_{UE}$-$P5_{UE}$ has been successfully received or not.

[00019] Figure 4 is an example of a prior art system including an RNC, a Node B, a UE and their associated buffers. This example assumes that the UE is the receiving entity and the Node B is the transmitting entity. In this prior art system, a PDU with SN = 3 is not received successfully by the UE. Therefore, the RLC in the UE requests its peer RLC layer in the RNC for a retransmission. Meanwhile, the PDUs with SNs = 6-9 are buffered in the Node B, and PDUs with SNs = 4 and 5 are buffered in the UE. It should be noted that although Figure 4 shows only several PDUs being buffered, in reality many more PDUs (such as 100 or more) and PDUs from other RLC entities may be buffered.

[00020] As shown in Figure 5, if a retransmission of the PDU with SN = 3 is required, it must wait at the end of the queue in the Node B buffer, and will be transmitted only after the PDUs with SNs = 6-9 are transmitted. The PDUs in the UE cannot be forwarded to the upper layers until all PDUs are received in sequence.

[00021] In this case, the PDU with SN = 3 stalls the forwarding of subsequent PDUs to higher layers, (i.e. SNs = 4-9), assuming all the PDUs are transmitted successfully. Again, it should be noted that this example only reflects 11 PDUs, whereas in normal operation hundreds of PDUs maybe scheduled in advance of retransmitted data PDUs, which further aggravates transmission latency and data buffering issues.

[00022] It would be desirable to have a system and method whereby the retransmitted data can avoid the delays due to congestion in the transmission buffers.

[00023] SUMMARY

[00024] The present invention is a system and method for transferring data in a wireless communication system. A plurality of data blocks are received and temporarily stored in a first memory. The plurality of data blocks are then transmitted. A determination is then made as to whether each of the transmitted data blocks was received successfully or needs to be retransmitted because the data block was not received successfully. Each of the transmitted data blocks that needs to be retransmitted is marked and stored in a second memory having a higher priority than the first memory. The marked data blocks stored in the second memory are transmitted before transmitting data blocks stored in the first memory.

[00025] Each marked data block may include a common channel priority indicator (CmCH-Pi). The CmCH-Pi of the marked data block is read and used to determine which of a plurality of memories to place the marked data block in based on the CmCH-Pi.

[00026] In accordance with one preferred embodiment of the present invention, a wireless communication system for transferring data includes a UE, a Node B in communication with the UE and a radio network controller (RNC) in communication with the Node B and the UE. The RNC transmits a plurality of data blocks to the UE via the Node B. The UE sends a status report to the RNC. The report indicates whether each of the transmitted data blocks was received successfully by the UE or needs to be retransmitted because the data block was not received successfully by the UE. The RNC marks each of the data blocks that needs to be retransmitted and sends the marked data blocks to the Node B. The Node B receives, temporarily stores and prioritizes transmission of the marked data blocks over other data blocks previously received and stored in Node B. The Node B transmits the marked data blocks to the UE before the other data blocks.

[00027] BRIEF DESCRIPTION OF THE DRAWINGS

[00028] A more detailed understanding of the invention may be had from the following description, given by way of example and to be understood in conjunction with the accompanying drawings wherein:

[00029] Figure 1 is a UTRAN MAC-hs.

[00030] Figure 2 is a prior art UE MAC-hs.

[00031] Figure 3 is a block diagram of the data flow between a Node B and a UE.

[00032] Figure 4 is a diagram of the RLC layer exhibiting a missed PDU transmission.

[00033] Figure 5 is a diagram of retransmission by the RLC layer of the missed PDU transmission.

[00034] Figure 6 is a signal diagram of a method of prioritizing retransmissions in accordance with the present invention.

[00035] Figure 7 is a block diagram of the data flow between a Node B and a UE, whereby retransmissions are assigned to a higher priority queue.

[00036] Figure 8 is a block diagram of the data flow of a DSCH transmission scheduling PDUs with CmCH-Pi indications.

[00037] Figures 9 and 10 are diagrams of retransmission by the RLC layer of a missed PDU transmission in accordance with the present invention.

[00038] DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[00039] The preferred embodiments will be described with reference to the drawing figures where like numerals represent like elements throughout.

[00040] In describing the present invention, reference may be made to the terminology "buffer" and "memory." It is intended that these terms are equivalent, and are used to indicate a plurality of data blocks or PDUs in a successive queue.

[00041] In order to reduce the latency of an RLC layer retransmission, the present invention prioritizes a retransmission of a PDU over a subsequent PDU in the buffer of an intermediate node, such as a Node B for example.

[00042] In the downlink direction (data transmissions from serving RNC (SRNC) to UE), one source of the latency of the retransmissions is generated in applications that buffer in the UTRAN outside of the SRNC. For example, buffering for an application could occur in the Controlling RNC (CRNC) or in the Node B. In several applications, the RNC RLC sends the PDU to the MAC-d in the RNC which creates an MAC-d PDU which is sent to the CRNC and then Node B (note that in the case that a UE has not moved out of the cell coverage of the SRNC, the CRNC will be the same RNC, and therefore, any messages sent are internal. When the UE has moved out of cell coverage of the SRNC and the new CRNC is known as the Drift RNC (DRNC). For simplification, in both cases this RNC will be referred to as a CRNC).

[00043] Since the MAC-d PDU contains exactly 1 RLC PDU (plus other potential MAC information), a MAC-d PDU can be considered equivalent to a RLC PDU. Although, discussion of PDUs in the CRNC or the Node B in the present application refers to MAC-d PDUs (not RLC PDUs), they can be considered equivalent for the purpose of the present invention and the term PDU will be used hereinafter to refer to both.

[00044] To allow for continuous data flow, the PDUs from the RNC RLC are usually queued in buffers of the CRNC or Node B for a while, before they are transmitted to the UE and thus the peer RLC. As will be described in detail hereinafter, the presently inventive method of retransmitting data at a higher priority bypasses the buffering/queuing of data in the UTRAN.

[00045] One embodiment of the present invention is the RLC retransmissions from the Radio Network Controller (RNC) to the User Equipment (UE) of a system employing High Speed Downlink Packet Access (HSDPA). A method 100 for reducing the latency of retransmissions in accordance with the present invention is depicted in Figure 6. Figure 6 shows the communications between an RNC 102, a Node B 104 and a UE 106.

[00046] The RLC layer in the UE 106 generates a Status Report PDU (step 108) which indicates the status of received, (i.e., successfully transmitted), or missing PDUs, (i.e., unsuccessfully transmitted). This status report PDU is

transmitted (step 110) to the RNC 102. Once the RLC layer in the RNC 102 receives the Status Report PDU from its peer entity in the UE 106, the RNC 102 prepares the retransmission of the missed PDU (step 112).

[00047] The present invention implements a method to enable the Node B to distinguish the retransmitted PDU from other PDUs. In a first embodiment, the RNC 102 marks the retransmitted PDU by using a field of bits on its Frame Protocol (FP) overheads. The retransmitted PDU includes a CmCH-Pi which is updated (or increased) every time the PDU is sent (step 114) from the RNC 102 to the Node B 104. This permits the Node B 104 to track the number of times the PDU is sent and, therefore, identify the proper queue in which to place the PDU. Preferably, the CmCH-Pi is typically set and updated at the RNC 102. However, this function may also be performed at the Node B 104. The Node B 104 reads the CmCH-Pi and determines the proper priority queue for the PDU (steps 116). The Node B 104 transmission scheduler services the higher priority queues in advance of lower priority queues. The Node B 104 places the PDU to be retransmitted in a buffer having a higher priority than it originally had when the PDU was originally transmitted as a result of the setting of the CmCH-Pi by the RNC 102.

[00048] The PDU is then retransmitted (step 118) in a buffer (i.e., memory) having a higher priority than the priority of the original transmission. Other transmissions for this UE may be buffered in Node B 104 lower priority transmission queue at the time of the PDU retransmission. The setting of the increased CmCH-Pi for retransmitted PDUs results in transmission scheduling in advance of other PDUs previously received and buffered in Node B 104.

[00049] Referring to Figure 7, retransmissions are assigned to a higher priority queue so that they supercede transmission of other data blocks which originate from the same "original" transmission buffer. Once the receiving H-ARQ processors $P1_{UE}$-$P5_{UE}$ process each data block, they are forwarded to the reordering buffers R_1, R_2, R_3 based on their priority; one reordering buffer for each priority level of data. For example, reordering buffer R_2 reorders data blocks $B2_1$, $B2_2$ and $B2_4$. Reordering buffer R_3 reorders data blocks $B3_3$, $B3_4$ and $B3_6$. A

data block ("X") is missing between the data blocks $B2_2$ and $B2_4$. An additional data block ("X") is missing between the data blocks $B3_4$ and $B3_6$. Thus, expected data blocks $B2_3$ and $B3_5$ are not received, e.g., due to a NACK message being misinterpreted as being an ACK message.

[00050] The missing data blocks are then retransmitted. Normally, the data block $B2_3$ would have been placed in the Priority 2 transmission buffer. However, since the data block $B2_3$ was missed and had to be retransmitted, the data block $B2_3$ is placed in a higher priority transmission buffer, (in this case the Priority 1 transmission buffer), and thus is sent earlier than if it were placed in the Priority 2 or 3 transmission buffers. Likewise, the data block $B3_5$ would have normally been placed in the Priority 3 transmission buffer. However, since the data block $B3_5$ was missed and had to be retransmitted, the data block $B3_5$ is placed in either the Priority 1 or Priority 2 transmission buffer so that it is transmitted earlier than if it had been placed in the Priority 3 transmission buffer.

[00051] Upon reception of PDUs in the Node B, the CmCH-PI is used to determine the priority queue B1n-B3n. The scheduler services the higher priority queues first and assign transmissions to transmitting H-ARQ processors $P1_B$-$P5_B$, Upon successful transmission to the UE, the receiving H-ARQ processors $P1_{UE}$ -$P5_{UE}$ forward the retransmitted PDUs to the RLC layer.

[00052] This procedure may also be applied for a DSCH system, except that the intermediate node is the CRNC instead of the Node B. Referring to Figure 8, PDUs 805 with CmCH-Pi indications are given priority by a prioritization entity 810 and are scheduled for transmission by the MAC-sh in the CRNC. The MAC-sh maintains multiple priority queues 815A, 815B, and a DSCH transmission scheduler 820 determines which PDU 805 is to be transmitted based on the priority of that data. Therefore, by setting increased CmCH-Pi for DSCH retransmissions, these transmissions will be serviced in advance of other data for the UE. This is similar to the HS-DSCH case where the Node B MAC-hs entity schedules transmissions.

[00053] Referring to Figure 9, a system is shown in accordance with the present invention implementing the prioritization method of Figure 6. After the RLC

layer in the UE transmits a status report PDU to the RLC layer in the RNC indicating that the PDU with SN = 3 has not been successfully received, the RNC sends a retransmission of the PDU with SN = 3. The PDU will be prioritized over other PDUs in the buffer of the intermediate node by placement within a higher priority buffer. It should be noted that although only 11 PDUs are shown, in actuality, there may be hundreds of queued PDUs.

[00054] The benefits of the present invention can be seen with reference to Figure 10, which depicts the result of the prioritization function in the receiving buffer. The retransmitted PDU with SN = 3 arrives at the receiving buffer, and the in-sequence PDUs with SN = 3 to 5 can be forwarded to the higher layer much more quickly than the prior art scenario depicted in Figure 5.

[00055] While the present invention has been described in terms of the preferred embodiment, other variations which are within the scope of the invention as outlined in the claims below will be apparent to those skilled in the art.

* * *

CLAIMS

What is claimed is:

1. A method for transferring data in a wireless communication system, the method comprising:

(a) receiving and temporarily storing a plurality of data blocks in a first memory;

(b) transmitting the plurality of data blocks;

(c) determining whether each of the transmitted data blocks was received successfully or needs to be retransmitted because the data block was not received successfully;

(d) marking each of the transmitted data blocks that needs to be retransmitted;

(e) temporarily storing the marked data blocks in a second memory having a higher priority than the first memory; and

(f) transmitting the marked data blocks stored in the second memory before transmitting data blocks stored in the first memory location.

2. The method of claim 1 wherein the data blocks are transmitted over a high speed downlink shared channel.

3. The method of claim 1 wherein at least one of the data blocks includes a plurality of multiplexed protocol data units (PDUs).

4. The method of claim 1 wherein each data block is a protocol data unit (PDU).

5. The method of claim 1 further comprising:

(g) assigning a unique transmission sequence number (TSN) to each of the data blocks.

6. The method of claim 1 further comprising:

(g) assigning a priority based on a required transmission latency for each of the data blocks.

7. The method of claim 1 wherein each marked data block includes a common channel priority indicator (CmCH-Pi), the method further comprising:

(g) reading the CmCH-Pi of the marked data block and determining which of a plurality of memories to place the marked data block in based on the CmCH-Pi.

8. A wireless communication system for transferring data, the system comprising:

(a) at least one user equipment (UE);

(b) a Node B in communication with the UE; and

(c) a radio network controller (RNC) in communication with the Node B and the UE, wherein:

(i) the RNC transmits a plurality of data blocks to the UE via the Node B;

(ii) the UE sends a status report to the RNC, the report indicating whether each of the transmitted data blocks was received successfully by the UE or needs to be retransmitted because the data block was not received successfully by the UE;

(iii) the RNC marks each of the data blocks that needs to be retransmitted and sends the marked data blocks to the Node B;

(iv) the Node B receives, temporarily stores and prioritizes transmission of the marked data blocks over other data blocks previously received and stored in the Node B; and

(v) the Node B transmits the marked data blocks to the UE before the other data blocks.

9. The system of claim 8 wherein the data blocks are transmitted over a high speed downlink shared channel.

10. The system of claim 8 wherein at least one of the data blocks includes a plurality of multiplexed protocol data units (PDUs).

11. The system of claim 8 wherein each data block is a protocol data unit (PDU).

12. The system of claim 8 wherein the Node B further comprises:

(b1) means for assigning a unique transmission sequence number (TSN) to each of the data blocks.

13. The system of claim 8 wherein the Node B further comprises:

(b1) means for assigning a priority based on a required transmission latency for each of the data blocks.

14. The system of claim 8 wherein each marked data block includes a common channel priority indicator (CmCH-Pi), the Node B further comprising:

(b1) means for reading the CmCH-Pi of the marked data block; and

(b2) means for determining which of a plurality of memories to place the marked data block in based on the CmCH-Pi.

15. A wireless communication system for transferring data in a wireless communication system, the system comprising:

(a) means for receiving and temporarily storing a plurality of data blocks in a first memory;

(b) means for transmitting the plurality of data blocks;

(c) means for determining whether each of the transmitted data blocks was received successfully or needs to be retransmitted because the data block was not received successfully;

(d) means for marking each of the transmitted data blocks that needs to be retransmitted;

(e) means for temporarily storing the marked data blocks in a second memory having a higher priority than the first memory; and

(f) means for transmitting the marked data blocks stored in the second memory before transmitting data blocks stored in the first memory location.

16. The system of claim 15 wherein the data blocks are transmitted over a high speed downlink shared channel.

17. The system of claim 15 wherein at least one of the data blocks includes a plurality of multiplexed protocol data units (PDUs).

18. The system of claim 15 wherein each data block is a protocol data unit (PDU).

19. The system of claim 15 further comprising:

(g) means for assigning a unique transmission sequence number (TSN) to each of the data blocks.

20. The system of claim 15 further comprising:

(g) means for assigning a priority based on a required transmission latency for each of the data blocks.

21. The system of claim 15 wherein each marked data block includes a common channel priority indicator (CmCH-Pi), the system further comprising:

(g) means for reading the CmCH-Pi of the marked data block; and

(h) means for determining which of a plurality of memories to place the marked data block in based on the CmCH-Pi.

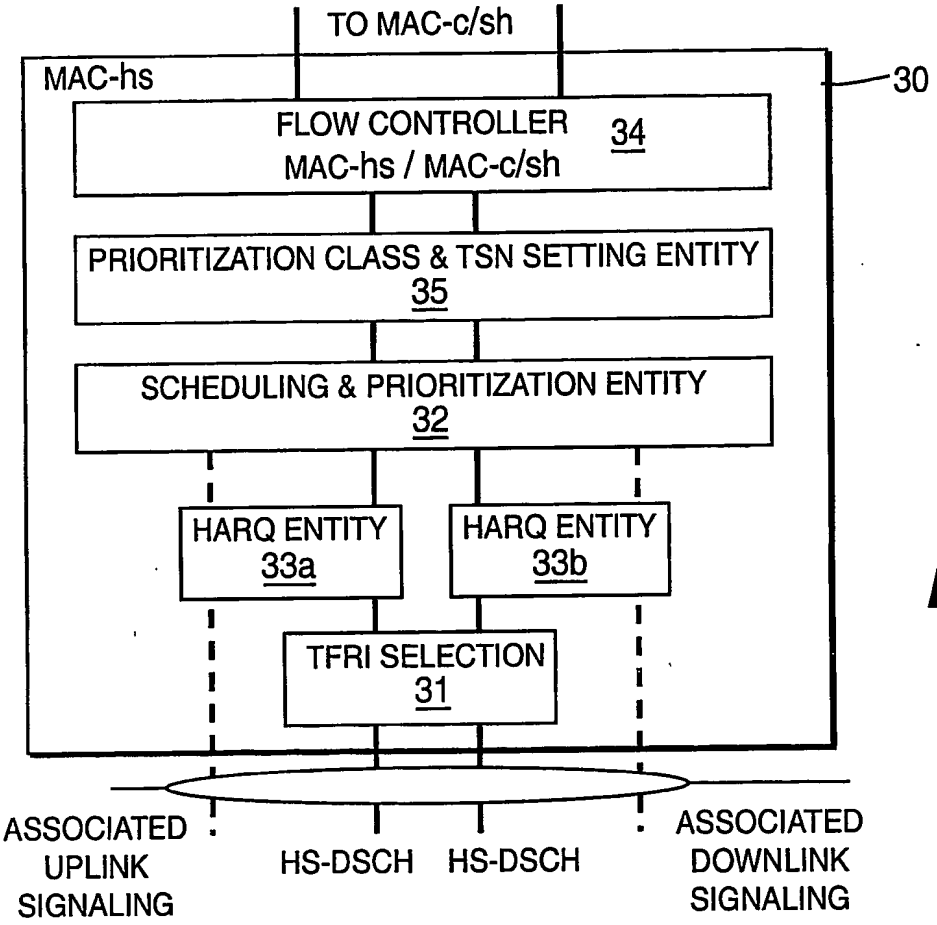


FIG. 1

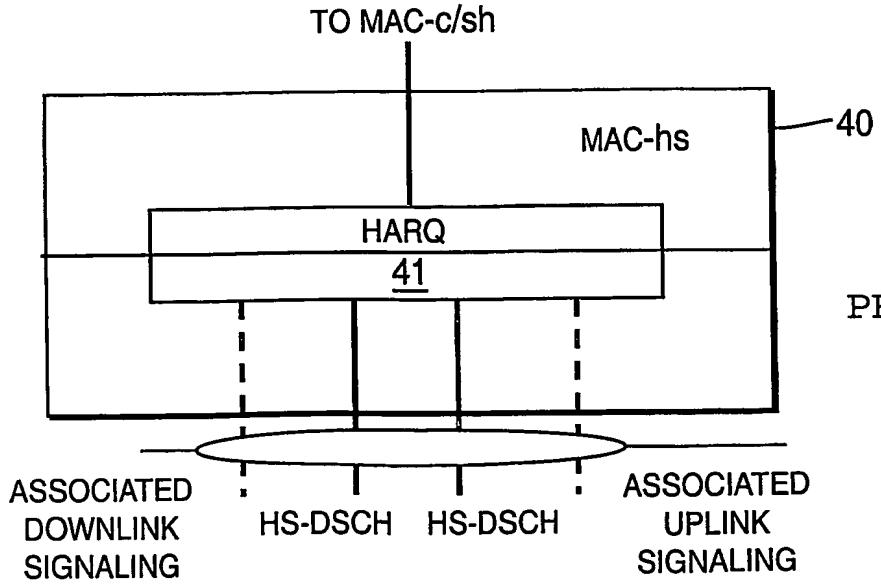


FIG. 2
PRIOR ART

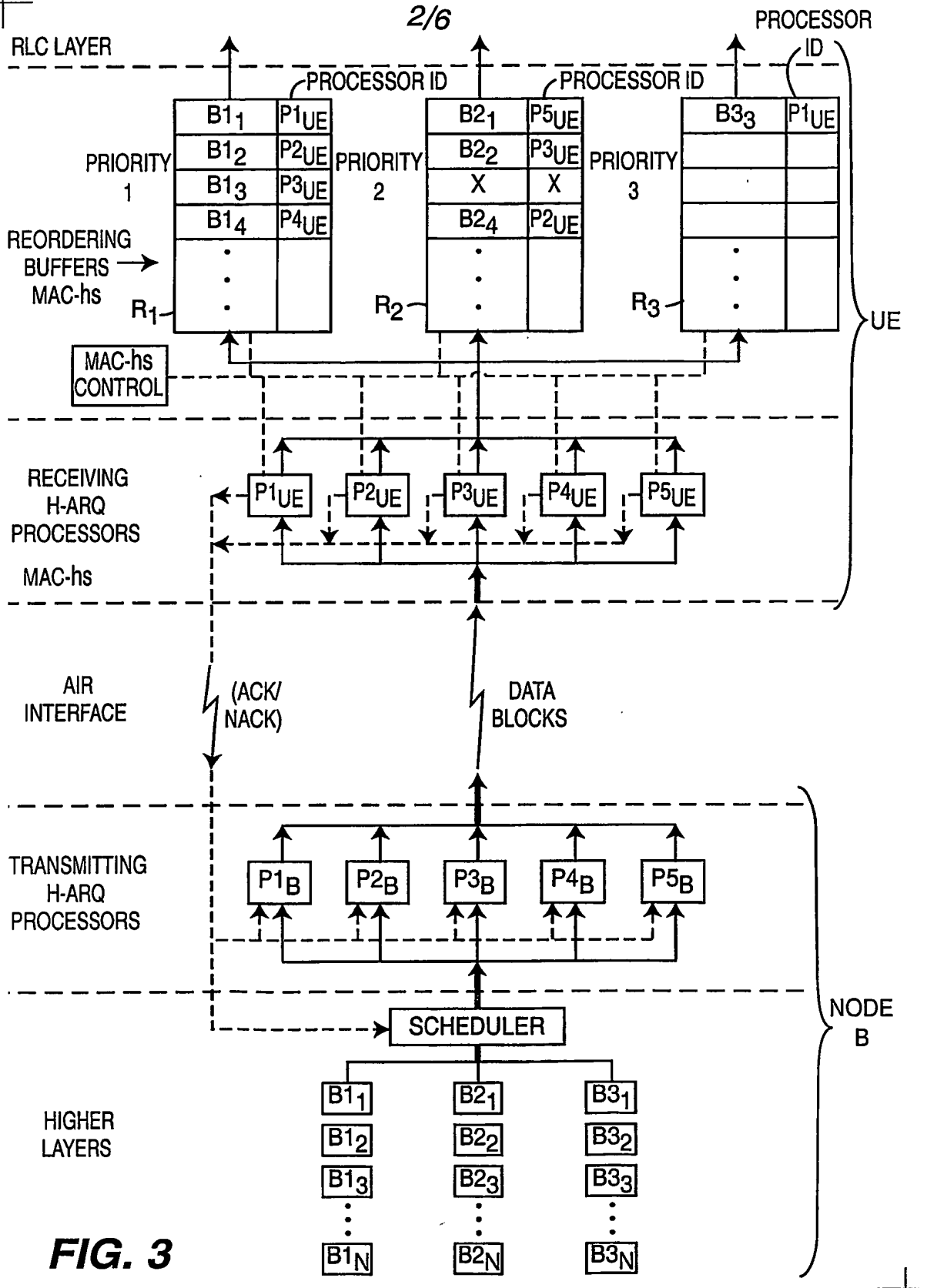

RLC LAYER
PROCESSOR ID
PROCESSOR ID
PROCESSOR ID
PRIORITY 1
PRIORITY 2
PRIORITY 3
REORDERING BUFFERS MAC-hs
R1
R2
R3
UE
MAC-hs CONTROL
RECEIVING H-ARQ PROCESSORS
MAC-hs
AIR INTERFACE
(ACK/ NACK)
DATA BLOCKS
TRANSMITTING H-ARQ PROCESSORS
SCHEDULER
NODE B
HIGHER LAYERS

FIG. 3

FIG. 4

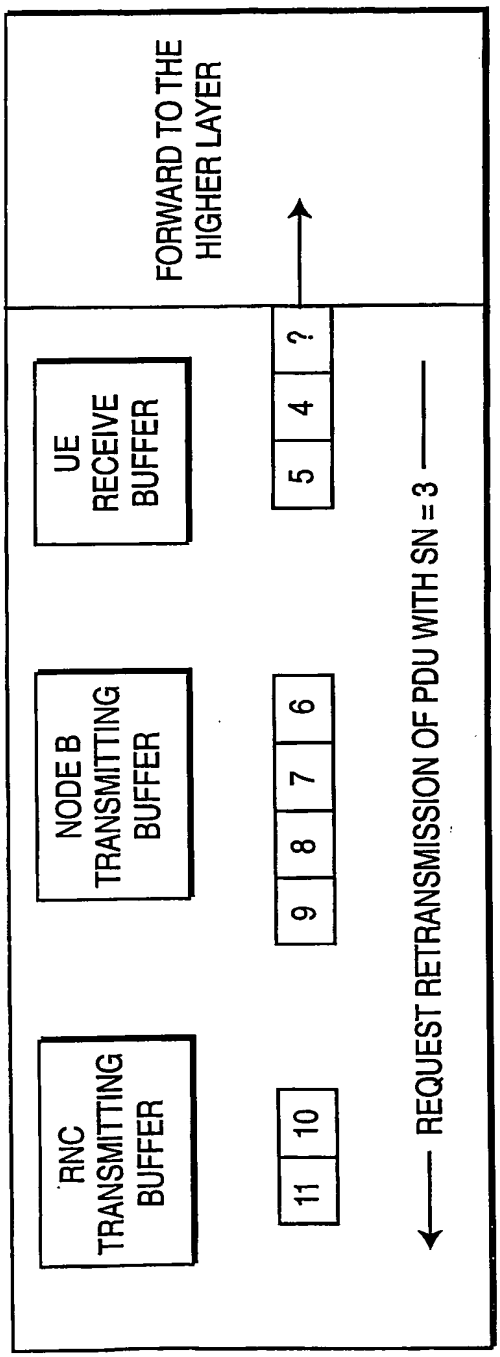
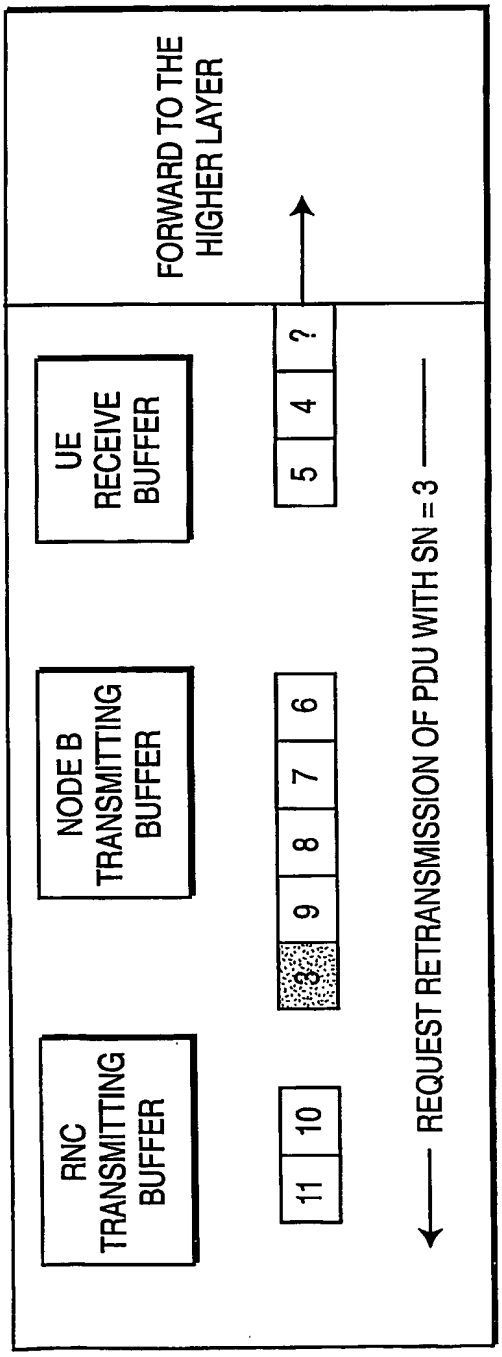

RNC TRANSMITTING BUFFER
NODE B TRANSMITTING BUFFER
UE RECEIVE BUFFER
FORWARD TO THE HIGHER LAYER
11
10
9
8
7
6
5
4
?
REQUEST RETRANSMISSION OF PDU WITH SN = 3

FIG. 5


RNC TRANSMITTING BUFFER
NODE B TRANSMITTING BUFFER
UE RECEIVE BUFFER
FORWARD TO THE HIGHER LAYER
11
10
9
8
7
6
5
4
?
REQUEST RETRANSMISSION OF PDU WITH SN = 3

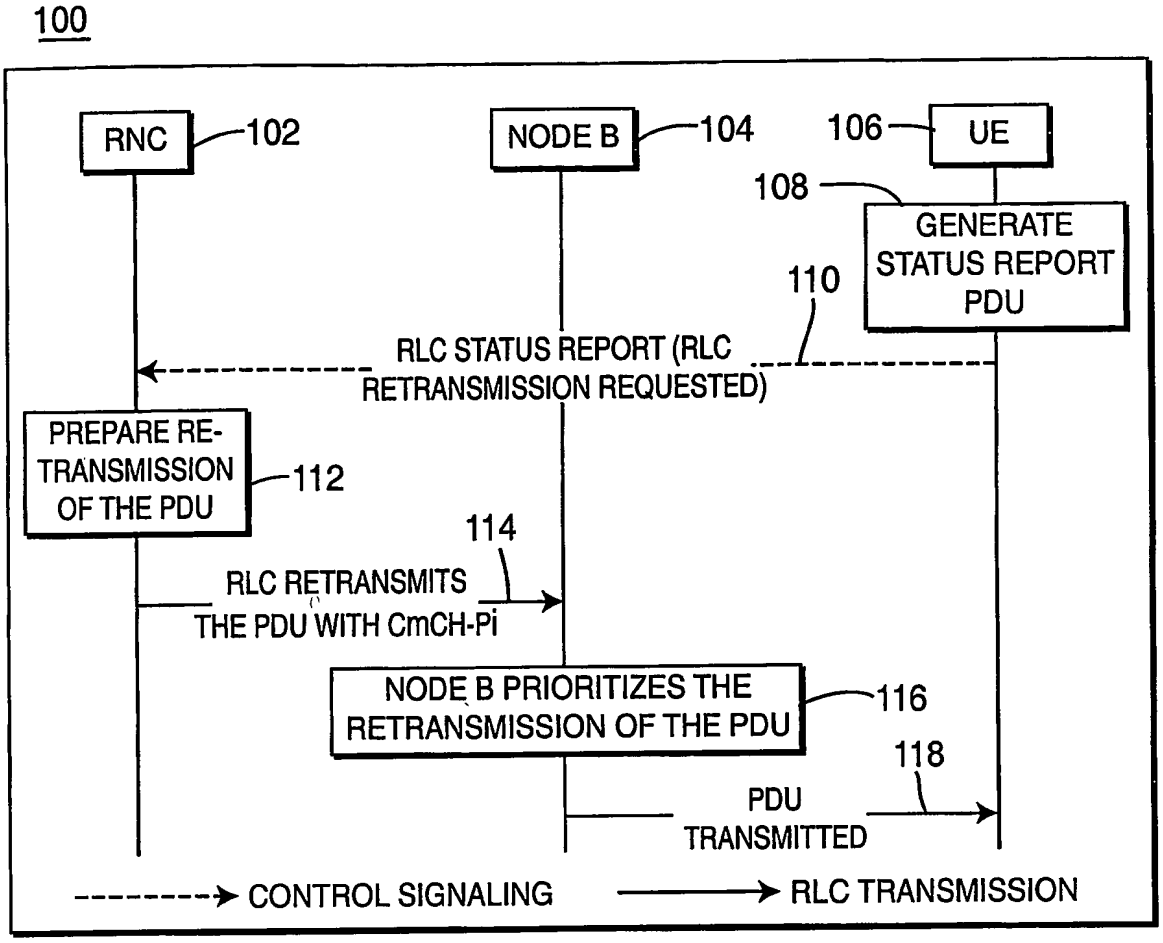
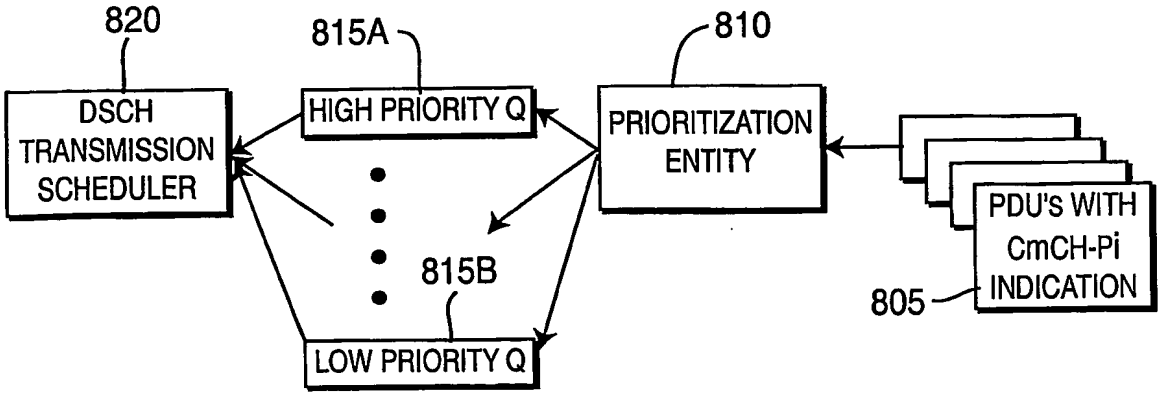


FIG. 6



DSCH PDU TRANSMISSION PRIORITY SCHEDULING

FIG. 8

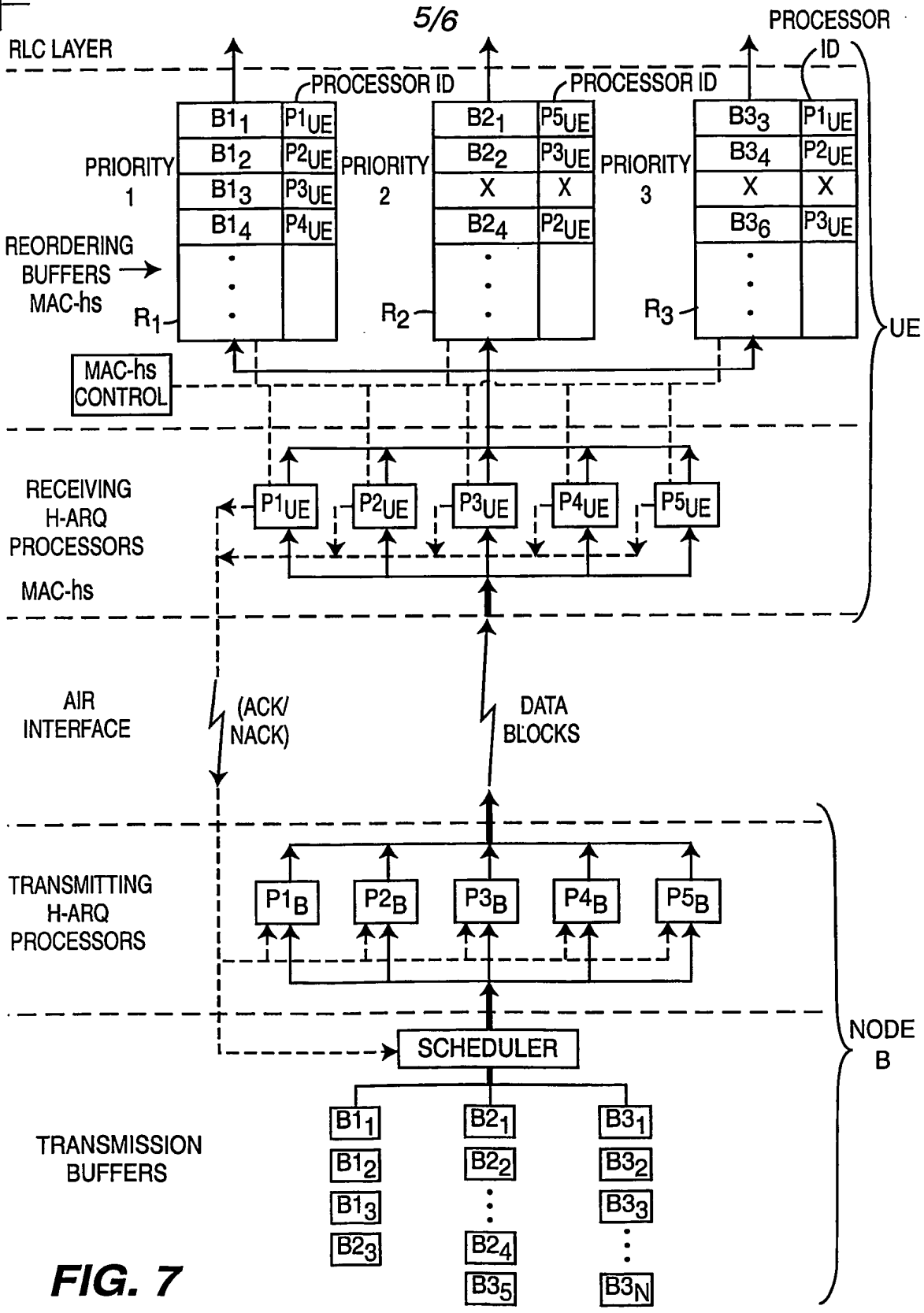

RLC LAYER
PROCESSOR ID
PROCESSOR ID
PROCESSOR ID
PRIORITY 1
PRIORITY 2
PRIORITY 3
B11 P1UE
B12 P2UE
B13 P3UE
B14 P4UE
B21 P5UE
B22 P3UE
X X
B24 P2UE
B33 P1UE
B34 P2UE
X X
B36 P3UE
REORDERING BUFFERS MAC-hs
R1
R2
R3
UE
MAC-hs CONTROL
RECEIVING H-ARQ PROCESSORS
P1UE P2UE P3UE P4UE P5UE
MAC-hs
AIR INTERFACE
(ACK/ NACK)
DATA BLOCKS
TRANSMITTING H-ARQ PROCESSORS
P1B P2B P3B P4B P5B
SCHEDULER
NODE B
TRANSMISSION BUFFERS
B11 B12 B13 B23
B21 B22 B24 B35
B31 B32 B33 B3N

FIG. 7

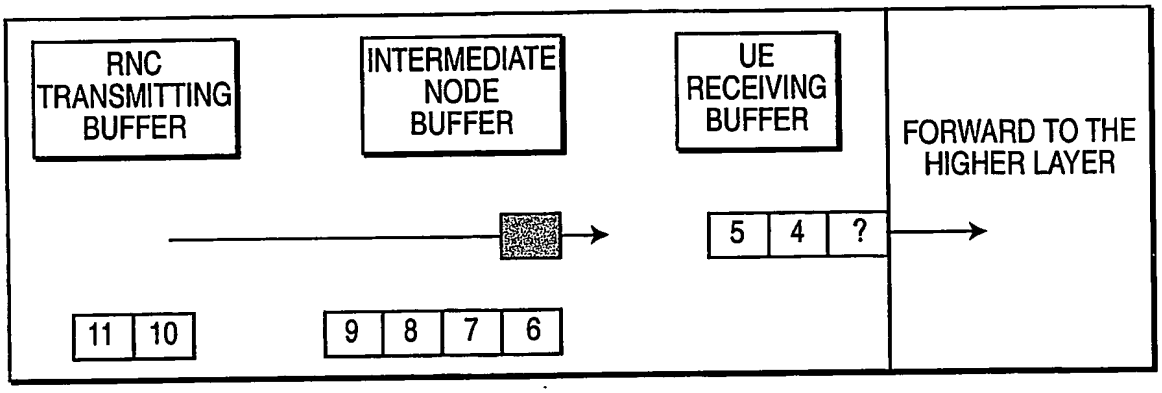

RNC TRANSMITTING BUFFER
INTERMEDIATE NODE BUFFER
UE RECEIVING BUFFER
FORWARD TO THE HIGHER LAYER
5
4
?
11
10
9
8
7
6

FIG. 9

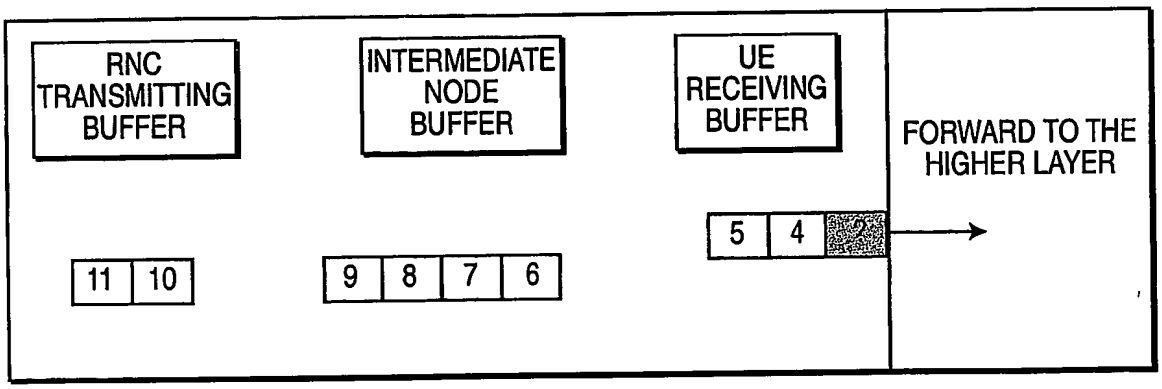

RNC TRANSMITTING BUFFER
INTERMEDIATE NODE BUFFER
UE RECEIVING BUFFER
FORWARD TO THE HIGHER LAYER
5
4
11
10
9
8
7
6

FIG. 10